ABSTRACT OF THE DISCLOSURE

The invention provides a program conversion apparatus which performs parallelization for a multi-thread microprocessor on an intermediate program level. A parallelization apparatus of the program conversion apparatus includes a fork spot determination section, a register allocation section and an instruction reordering section. The fork spot determination section determines a fork spot and a fork system based on a result of a register allocation trial performed by the register allocation section, the number of spots at which memory data dependence is present, and branching probabilities and a data dependence occurrence frequency obtained from a profile information file. The instruction reordering section reorders instructions preceding to and succeeding the FORK instruction in accordance with the determination.